A GaAs MMIC MMDS Downconverter

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Abstract We present design and performance of a new GaAs MMDS downconverter IC. The IC consists of an integrated mixer, VCO, and buffer amp on a single GaAs die. The downconverter is designed for use in an MMDS receiver converting a block of 32 analog TV channels in the 2500 - 2686 MHz band to an IF in the 200 - 400 MHz range.

Introduction

MMDS TV, or "wireless cable" as it is also known, is a multichannel broadcast service that delivers cable network video to subscribers using microwave frequencies in the 2500 - 2686 MHz band [1]. Currently, 32 analog TV channels are available on MMDS systems, although digital systems with 10:1 compression have been demonstrated. Recently, there has been increased interest in MMDS as an alternative broadband information link to the home [2].

In this paper we describe the design and performance a GaAs downconverter IC for an MMDS receiver module. The downconverter is designed to be used in a receiver system with an LNA which provides gain and sets the noise figure, as shown in Figure 1. An overview of MMDS receivers is given in [3].

The downconverter IC contains a balanced mixer, a VCO and a LO buffer amp. The downconverter was designed and fabricated using Motorola's ion implanted MMIC-C process. This process is designed to be low cost and highly manufacturable [4]. The downconverter is packaged in a standard 16 pin SOIC plastic package.

Circuit Design

Design specifications for the IC are shown in Table 1. These specifications are compatible with those associated with the discrete solution described in [3]. All circuit simulation was performed using the HP MDS non-linear microwave simulator.

The mixer used is shown in Figure 2. This is a double balanced design, consisting of a FET quad, driven by a differential amplifier which amplifies the RF signal. The LO

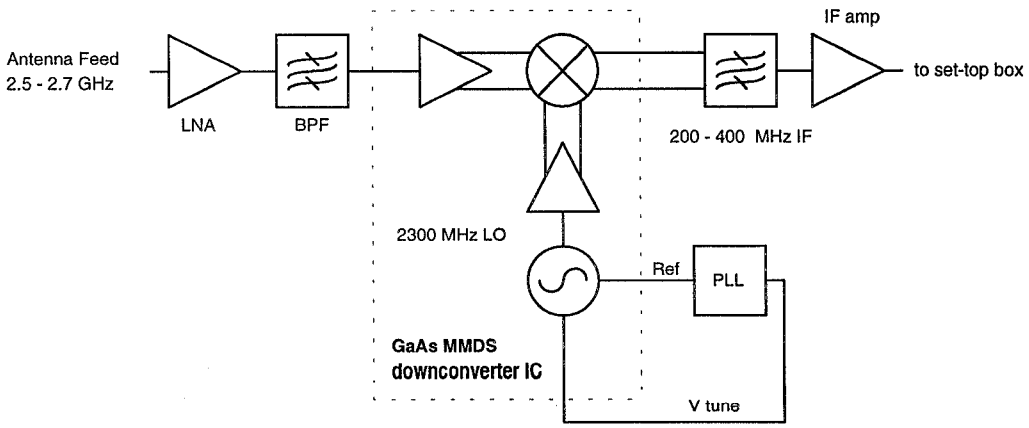

Figure 1. Block diagram of a typical receiver using the MMDS downconverter.

signal is injected differentially into the gates of the FET quad. This design was chosen for its high IP3, broadband operation, and relatively low noise performance. The mixer provides a differential output.

In this design, the current source for the differential amplifier is replaced by an inductor, which provides a high impedance at the RF. Source degeneration inductors are also used to improve linearity without sacrificing voltage drop across the active devices. The difamp FETs are self biased, with the series resistance in the inductors used to help establish Vgs. This eliminates the need for a negative supply. The series inductance required for rf matching is partly supplied by the package inductance, and partly by an off-chip inductor.

RF range	2500 - 2700 MHz
IF range	100 - 500 MHz
LO range	2100 - 2500 MHz
Input IP3	+15 dBm
Gain	3 - 5 dB
noise figure	9 dB
Tuning voltage	1 - 9 V
VCO phase noise	-85 dBc/Hz @ 10 kHz
Supply	5V, 125 mA

Table 1. Performance Specifications for CATV up and down converters.

VCO phase noise is a critical parameter, especially for digital applications. Simulation of VCO phase noise is difficult, and these difficulties are compounded by its strong dependence on package parasitics and the external varactor. We began by measuring 1/f noise for the devices and using this information in the simulator. This proved to be less than successful, probably due more to the capabilities of the device model than to the simulator itself.

In the end, an empirical approach was taken. The circuit design chosen was a Clapp oscillator, shown in Figure 3, feeding a differential buffer amplifier, shown in Figure 4. It was generally true that the VCO phase noise improved as the tank capacitor values increased, and also as the device width was increased. Also, it is very important to isolate the supply lines on the chip to eliminate noise coupled into the VCO. An external varactor in the VCO tank circuit was used to achieve the tuning range required.

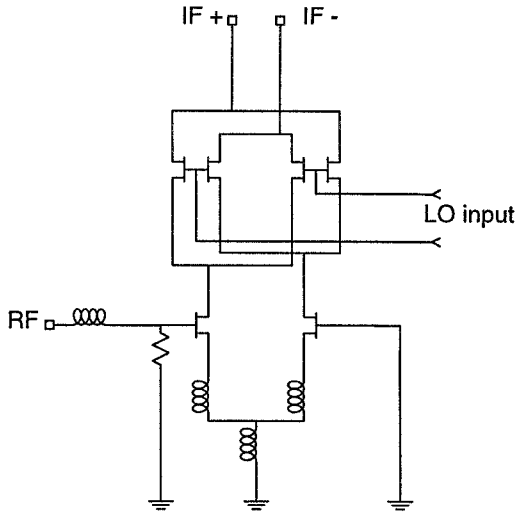

Figure 2. MESFET mixer.

VCO to buffer amp coupling is critical. The VCO signal is sampled at the gate of the MESFET, because the waveform here has both a high peak to peak swing and good spectral purity. However, coupling too strongly at this point will load the VCO, reducing it's tuning range and degrading phase noise. The input impedance of the LO bufferamp must also be kept as high as possible, by using the smallest possible

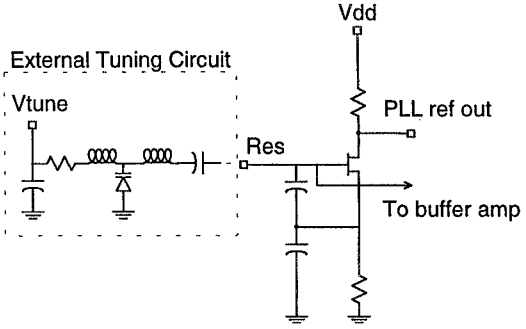

Figure 3. VCO and external tank circuit.

devices that will still deliver an acceptable signal level to the mixer gates.

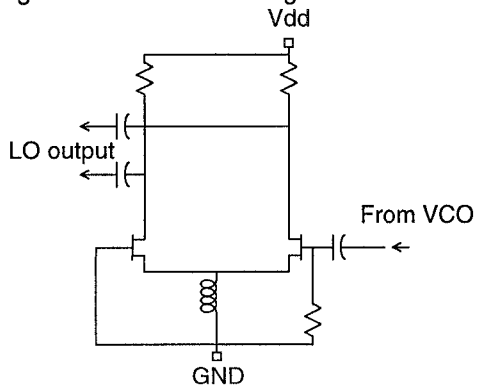

Figure 4. LO buffer amp.

The downconverter chip was designed using the HP MDS circuit simulator. The active devices were modeled using the Advanced Curtice model.

Package modeling was critical to the design of the IC. At 2.7 GHz, the SOIC-16 package electrical parasitic effects are significant, particularly the common lead inductance between package and PCB ground. A lumped element model of the package and wirebonds was used which accounted for mutual coupling between adjacent pins.

The die size of the downconverter GaAs IC is 40 x 60 mils.

Test

The IC was mounted on an FR-4 PCB and tested in a 50 ohm system. The test circuit is shown in Figure 5. An output combiner/bias network consisting of rf chokes, dc blocking capacitors, and a 1:1 transformer was used. A Toshiba 1sv239 varactor was used in the tank circuit.

Measured gain, noise figure, and input IP3 are shown in Figures 6 - 8 for 5 devices in the test fixture. The data are not corrected for fixture loss. Noise figure was measured using a 5% bandpass filter on the input to the downconverter. Without this filter, the measurements are optimistic by ~ 3 dB.

VCO phase noise for the downconverter was measured at -85 dBc/Hz @ 10 kHz offset in

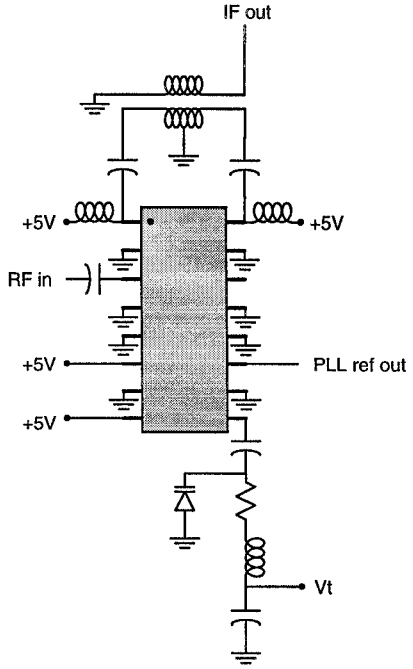

Figure 4. Downconverter test circuit.

free running. Typical phase noise suppression of 4 - 5 dB at 10 kHz offset is measured when the VCO is locked using a PLL. Suppression improves substantially as the offset frequency is reduced.

The downconverter used a total of 120 mA from a 5V supply.

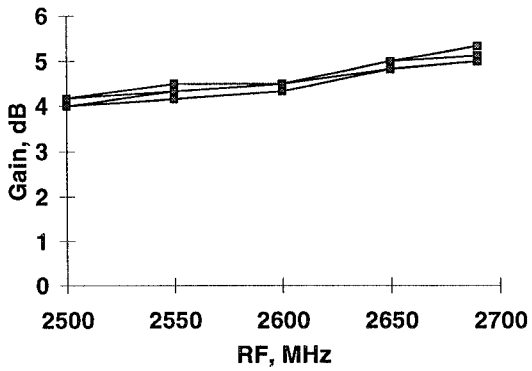

Figure 5. Conversion gain vs. input frequency

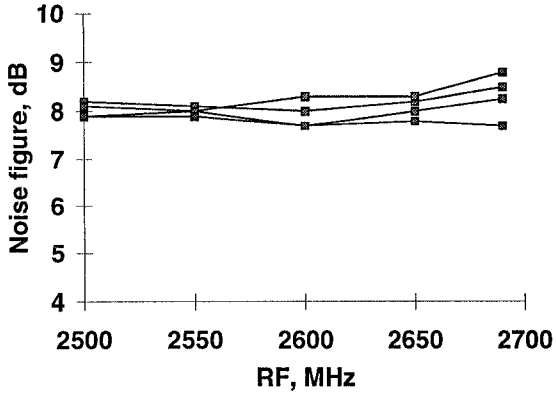

Figure 6. Noise figure vs. input frequency.

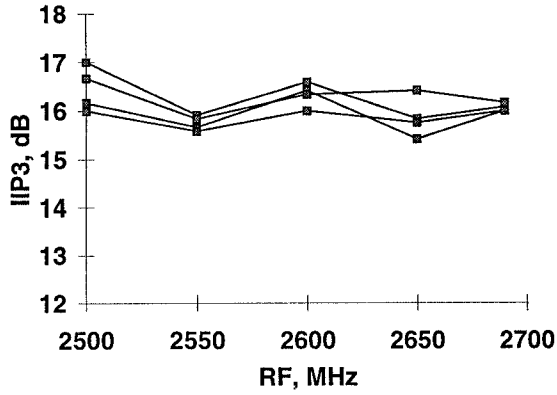

Figure 7. Input intercept point vs. input frequency

Conclusions

A new MMDS downconverter GaAs IC has been described. The IC will allow a significant parts reduction in MMDS receiver design. Performance of the IC is compatible with state of the art receiver design goals.

Acknowledgments

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